What is claimed is:

1. A fractional-spaced digital equalizer comprising:

a bank of register delay elements representing the data register bank that stores those samples of the input distorted waveform;

a switch S1 to control that portion of the joint ISI-canceling and MF equalizer update associated with the ISI-cancellation process;

a bank of register elements representing equalizer FF weight register bank that stores the equalizer FF weights coefficient values;

a bank of multiplier elements used in forming the inner products associated with both the ISI-cancellation and MF constraint updates;

a bank of summing nodes used in forming the inner products associated with both the ISI-cancellation and MF constraint updates;

an M:1 commutation device to perform decimation to the symbol rate;

an algorithm to form the error sequence associated with ISI cancellation;

an algorithm to convert the ISI cancellation error signal into an adjustment signal needed to control the equalizer FF weight update in accordance with the criterion for ISI cancellation;

an algorithm to update the contents of the equalizer FF weight register bank in accordance with first, the criterion for ISI-cancellation, and second, the MF constraint criterion;

a bank of register elements representing the constraint register bank to store samples of the constraint waveform;

an algorithm that generates samples of a constraint waveform;

a constraint waveform used in forming the inner product associated with the MF constraint processing;

a switch S2 to control that portion of the joint ISI-canceling and MF equalizer update associated with the MF constraint process;

a parameter β representing the constraint level of the MF constraint update;

a differencing node to subtract the orthogonality measure from the constraint level in order to form the constraint error; and

an algorithm to convert the constraint error signal into an adjustment signal needed to control the equalizer FF weight update in accordance with the MF constraint criterion;

2. The fractional-spaced equalizer as set forth in claim **1** wherein said equalizer operates at M-samples-per-symbol where $M > 1$ and satisfies the Nyquist Criterion.

3. The fractional-spaced equalizer as set forth in claim **2** wherein said sampling factor M is equal to 2.

4. The fractional-spaced equalizer as set forth in claim **1** wherein said equalizer operates as a complex equalizer comprising complex operations;

5. The fractional-spaced equalizer as set forth in claim **1** wherein said equalizer operates as a real equalizer comprising real operations;

6. The fractional-spaced equalizer as set forth in claim **1** wherein the signal occurring prior to said M-to-1 decimator is passed directly to switch S2, instead of passing through said M-to-1 commutator, so that constraint processing can be performed using every fractional-spaced sample of the distorted input waveform;

7. The fractional-spaced equalizer as set forth in claim **1** wherein said algorithm that computes the error associated with ISI-cancellation is based upon a training sequence update and comprises:

a training sequence of distortion-less data; and

a differencing node to form the difference between the equalized decimated signal and the training sequence;

8. The fractional-spaced equalizer as set forth in claim **1** wherein said algorithm that computes the error associated with ISI cancellation is based upon a decision-directed update and comprises:

a slicer device to quantize samples of equalized decimated signal; and

a differencing node to form the difference between pre-slicer sequence and post-slicer sequence;

9. The fractional-spaced equalizer as set forth in claim **1** wherein said algorithm that computes the error associated with ISI cancellation is based upon the blind CMA update and comprises:

an algorithm to form the statistical parameter R_m measuring the ratio of moments of the pre-pulse shaped modulation amplitudes;

a switch S7 to eliminate the computation of R_m from the processing so that parameter R_m is computed only one time;

a register element to store the value of parameter R_m;

a complex conjugation operator to conjugate the sample input to the CMA;

a multiplier element to obtain the product between the input sample and its complex conjugate;

a differencing node to form the difference between parameter R_m and the absolute value of the input sample squared; and

a multiplier element to obtain the product of (1) the difference between parameter R_m and the absolute value of the input sample squared and (2) the input sample;

10. The fractional-spaced equalizer as set forth in claim **9** wherein said algorithm forming the value R_m comprises:

an absolute value operator to perform an absolute value of the input modulated 2-tuple;

a divide operation to form the value of R_m;

a switch S8 to control when the numerator portion of a ratio is to be delivered to the divide operation to form the value of parameter R_m;

a switch S9 to control when the denominator portion of a ratio is to be delivered to the divide operation to form the value of parameter R_m;

a counter to control when switches S8 and S9 are closed to form the value of parameter R_m;

a summing node used in the ratio's numerator accumulation process;

a summing node used in the ratio's denominator accumulation process;

a register element used in the ratio's numerator accumulation process;

a register element used in the ratio's denominator accumulation process;

a squaring operator;

a operator to perform a power operation to the m-th power; and

a parameter m representing the statistical moment of

the CMA update satisfies the condition $m > 0$;

11. The fractional-spaced equalizer as set forth in claim **1** wherein said algorithm converting the ISI cancellation error signal into an adjustment signal comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input error sequence;

a parameter μ to control the adaptation rate of the equalizer's weight in accordance with the criterion for ISI cancellation; and

a multiplier element to form the product of the conjugated error sequence and parameter μ;

12. The fractional-spaced equalizer as set forth in claim **11** wherein the value for said scalar μ is in the range $0 < \mu < \mu_{crit}$ and μ_{crit} is inversely proportional to the power level of the samples residing in the equalizer data register bank;

13. The fractional-spaced equalizer as set forth in claim **1** wherein said algorithm driving the equalizer weight update comprises:

a bank of multiplier elements to scale each element in the data register bank with a sample of the ISI cancellation adjustment signal; and

a bank of summing nodes to form the addition of the said bank of products with the current contents of the equalizer weight register bank;

14. The fractional-spaced equalizer as set forth in claim **1** wherein constraint waveform is defined to be a high frequency signal;

15. The fractional-spaced equalizer as set forth in claim **14** wherein said high frequency signal representing said constraint waveform is sinusoidal in nature;

16. The fractional-spaced equalizer as set forth in claim **15** wherein said high frequency sinusoid signal is a complex sinusoid of the form $A\ exp\{ j\ 2\pi f kT_s + \phi \}$;

17. The fractional-spaced equalizer as set forth in claim **16** wherein said frequency f is a time variable frequency;

18. The fractional-spaced equalizer as set forth in claim **17** wherein minimum and maximum values of said time-variable frequency are selected to develop a robust out-of-band spectral mask for the FSE that is comparable to that of a MF.

19. The fractional-spaced equalizer as set forth in claim **16** wherein said amplitude A is an amplitude fixed to a singular value and satisfies $|A| > 0$;

20. The fractional-spaced equalizer as set forth in claim **16** wherein said amplitude A is a time variable amplitude A_s and satisfies $|A| > 0$;

21. The fractional-spaced equalizer as set forth in claim **16** wherein said phase ϕ is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$;

22. The fractional-spaced equalizer as set forth in claim **16** wherein said phase ϕ is a time variable phase and satisfies $\{0 \leq \phi < 2\pi\}$;

23. The fractional-spaced equalizer as set forth in claim **15** wherein said high frequency sinusoid signal is a real sinusoid, either of the form $A \, sin\{ 2\pi f kT_s + \phi \}$ or $A \, cos\{ 2\pi f kT_s + \phi \}$.

24. The fractional-spaced equalizer as set forth in claim **23** wherein said frequency f of said sinusoid is a time variable frequency;

25. The fractional-spaced equalizer as set forth in claim **24** wherein minimum and maximum values of said time-variable frequency f are selected to develop a robust out-of-band spectral mask for the FSE that is comparable to that of a MF.

26. The fractional-spaced equalizer as set forth in claim **23** wherein said amplitude A is an amplitude fixed to a singular value and satisfies $|A| > 0$;

27. The fractional-spaced equalizer as set forth in claim **23** wherein said amplitude A is a time variable amplitude A_s and satisfies $|A| > 0$;

28. The fractional-spaced equalizer as set forth in claim **23** wherein said phase ϕ is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$;

29. The fractional-spaced equalizer as set forth in claim **23** wherein said phase ϕ is a time variable phase and satisfies $\{0 \leq \phi < 2\pi\}$;

30. The fractional-spaced equalizer as set for in claim **1** wherein said algorithm generating said constraint waveform comprises:

an overflow counter to generate an integer i that indexes a frequency register bank;

a frequency register bank storing the independent frequencies of the sinusoidal signal representing the constraint waveform;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a parameter N representing the number of independent constraint frequencies;

a summing node to increment the count of the overflow counter; and

a quadrature oscillator that generates samples of the sinusoidal signal representing the constraint waveform from the frequencies in the frequency register bank;

31. The fractional-spaced equalizer as set for in claim **1** wherein samples of said constraint waveform are loaded into the constraint register bank via ROM lookup table;

32. The fractional-spaced equalizer as set forth in claim **1** wherein value of said constraint level parameter β resides in the range $\{0 \leq \beta < 1\}$.

33. The fractional-spaced equalizer as set forth in claim **1** wherein said differencing node forming constraint error is eliminated from the architecture of the present invention when parameter β is set to 0.

34. The fractional-spaced equalizer as set forth in claim **1** wherein said MF error adjustment algorithm comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input MF constraint error;

a parameter α to control the adaptation rate of the equalizer's weight in accordance with the MF constraint criterion; and

a multiplier element to form the product of the complex conjugate MF constraint error and parameter α;

35. The fractional-spaced equalizer as set forth in claim **34** wherein the value for said scalar α satisfies $\alpha > 0$;

36. The fractional-spaced equalizer as set forth in claim **34** wherein the value for said scalar α is equal to A/L commensurate with the constraint waveform defined as a sinusoidal signal of amplitude A and length L;

37. The fractional-spaced equalizer as set forth in claim **1** where said fractional-spaced equalizer further comprises an algorithm that modifies the constraint waveform via time domain windowing;

38. The fractional-spaced equalizer as set forth in claim **36** wherein said algorithm that modifies the constraint waveform via time domain windowing does so with a single window function;

39. The fractional-spaced equalizer as set forth in claim **38** wherein said an algorithm that modifies the constraint waveform via time domain windowing with a single window function comprises:

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a window function;

a set of coefficients representing a window function used to window the samples of the constraint sinusoid; and

a bank of register elements to store the set of coefficients representing the window function;

40. The fractional-spaced equalizer as set forth in claim **39** wherein said window function is derived from any function that can modify the time response of the constraint sinusoid through time-domain windowing;

41. The fractional-spaced equalizer as set forth in claim **40** wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function;

42. The fractional-spaced equalizer as set forth in claim **37** wherein said an algorithm that modifies the constraint waveform via time domain windowing does so with multiple window functions;

43. The fractional-spaced equalizer as set forth in claim **42** wherein said an algorithm that modifies the constraint waveform via time domain windowing with multiple window functions comprises:

a register bank to store the samples of the current state of the windowed constraint waveform during the multi-window process;

a switch S10 to load the pre-windowed constraint waveform into the register bank only one time;

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a particular window function of the set of window functions;

a collection of window functions used to window the samples of the constraint sinusoid;

a collection of banks of register elements to store the set of coefficients of the collection of window functions;

a switch S12 to allow the multiplier bank to access a particular window function of the set of window functions; and

a switch S11 to deliver the windowed constraint waveform to the constraint register bank when the windowing process has been completed;

44. The fractional-spaced equalizer as set forth in claim **43** wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function.

45. The fractional-spaced equalizer as set forth in claim **1** where said fractional spaced equalizer further comprises an algorithm that controls the rate at which the contents of the equalizer's FF weight register bank are updated in accordance with the MF constraint update;

46. The fractional-spaced equalizer as set forth in claim **45** where said algorithm that controls the rate at which the contents of the equalizer's FF weight register bank are updated in accordance with the MF constraint criterion comprises:

a switch S3 to control when the algorithm for updating the contents of the equalizer FF weight registers is to be engaged;

an overflow counter to control when switch S3 is to be open and closed;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

a summing node to increment the count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a switch S4 to allow the overflow test to use the value designated by parameter P0 as the maximum count value;

a switch S5 to allow the overflow test to use the value designated by parameter P1 as the maximum count value;

a switch S6 to allow the overflow test to use the value designated by parameter P2 as the maximum count value;

a parameter P0 that represents a maximum count value;

a parameter P1 that represents a maximum count value; and

a parameter P2 that represents a maximum count value;

47. The fractional-spaced equalizer as set forth in claim **46** wherein said parameter P0, P1, and P2 are integers and satisfy P0 > 0, P1 > 0, and P2 > 0;

48. The fractional-spaced equalizer as set forth in claim **1** wherein said fractional spaced equalizer further comprises an algorithm that initializes the contents of the equalizer's FF weight register bank with coefficients of RRC MF;

49. The fractional-spaced equalizer as set forth in claim **48** where said algorithm that initializes the contents of the equalizer's FF weight register bank with coefficients of a RRC MF comprises:

a selected set of RRC MF coefficients loaded from ROM into the register positions of the equalizer FF weight register bank; and

a switch S13 to shutoff the initialization after the contents of the equalizer FF weight register bank;

50. The fractional-spaced equalizer as set forth in claim **1** where said fractional-spaced equalizer further comprises a decision-feedback update;

51. The fractional-spaced equalizer as set forth in claim **50** where said decision-feedback update comprises:

a register delay bank to store past decisions from a slicer device;

a slicer device to quantize samples of equalized decimated signal;

a register bank representing the decision register bank that stores the values of the weights of a decision-feedback filter;

a bank of multiplier elements used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a bank of summing nodes used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a single summing node adding the decision register and decision-feedback weight inner product to the output of the M:1 commutator;

a bank of multiplier elements used in updating the contents of the decision-feedback weight register bank;

a bank of summing nodes in updating the contents of the decision-feedback weight register bank;

52. A method of performing the inner product computation associated with the MF constraint criterion, the method comprising the steps of:

using only the L_w central multiplier elements of the multiplier bank, where $L_w < L$, to multiply only L_w central samples of the constraint waveform with the contents of only the L_w central registers of the equalizer FF weight register bank; and

using only the L_w central summing nodes of the bank of summing nodes, where $L_w < L$, to add up the L_w products formed from multiplication of only the L_w central samples of the constraint waveform with the contents of only the L_w central registers of the equalizer FF weight register bank;

53. A fractional-spaced digital equalizer comprising:

a set of M banks of register delay elements representing data sub-register banks $\underline{u}_0$, $\underline{u}_1$, ... $\underline{u}_{(M-1)}$ that store those samples of the input distorted waveform which are commutated to data sub-register banks $\underline{u}_0$, $\underline{u}_1$, ..., $\underline{u}_{(M-1)}$;

a set of M banks of register elements representing the equalizer FF weight sub-register banks $\underline{w}_0$, $\underline{w}_1$, ..., $\underline{w}_{(M-1)}$ that store the values of the equalizer's FF weights, with each bank storing a different subset of the total weight set;

a set of M banks of register elements representing constraint sub-register banks $\underline{c}_0, \underline{c}_1, \ldots \underline{c}_{(M-1)}$ that store samples of the constraint waveform;

an algorithm that generates samples of a constraint waveform;

a constraint waveform used in forming the inner product associated with the MF constraint processing;

a commutator COM 1 which delivers samples of the

input distorted waveform to be equalized to data sub-register banks $\underline{u}_0, \underline{u}_1, \ldots \underline{u}_{(M-1)}$;

a switch S1 to control that portion of the joint ISI-canceling and MF equalizer update associated with the ISI-cancellation process;

a bank of multiplier elements used in forming the inner products associated with both the ISI-cancellation and MF constraint updates;

a bank of summing nodes used in forming the inner products associated with both the ISI-cancellation and MF constraint updates;

a single register delay element to store the inner products associated with the formation of the equalized signal;

a switch S14 to control when the error sequence associated with ISI-cancellation is to be developed;

a switch S2 to control that portion of the time-multiplexing process associated with the MF constraint update;

a single register delay element to store an inner product computation associated with the MF constraint processing;

a switch S15 to control when the MF constraint error is to be developed;

a commutator COM 2 which controls which pair of sub-register banks, either $\{\underline{u}_0,\underline{c}_0\}$ or $\{\underline{u}_1,\underline{c}_1\} \ldots$ or $\{\underline{u}_{(M-1)},\underline{c}_{(M-1)}\}$, are to access the multiplier bank at the current COM 1 position;

a commutator COM 3 which controls which equalizer FF weight sub-register bank, either w_0 or w_1 ... or $w_{(M-1)}$ is to access the multiplier bank at the current COM 1 position;

a clock to control the adjustment of COM 1, COM 2, and COM 3;

a summing node to add the two inner product sums which form the equalized signal;

an algorithm to form the error sequence associated with ISI cancellation;

an algorithm to convert the ISI cancellation error signal into an adjustment signal needed to control the equalizer FF weight update in accordance with the criterion for ISI cancellation;

an algorithm to update the contents of the equalizer FF weight sub-register banks $\{\underline{w}_0, \underline{w}_1, \ldots, \underline{w}_{(M-1)}\}$ in accordance with first, the criterion for ISI-cancellation, and second, the MF constraint criterion;

a summing node to add the two inner product sums which form the measure of orthogonality between the equalizer's weights and constraint waveform;

a parameter β representing the constraint level of the MF processing;

a differencing node needed to subtract the orthogonality measure from the constraint level in order to form the constraint error;

an algorithm to convert the constraint error signal into an adjustment signal needed to control the equalizer FF weight update in accordance with the MF constraint criterion;

54. The fractional-spaced equalizer as set forth in claim **53** wherein said poly-phase configured equalizer accommodates a input signal sampled at M-samples-per-symbol by using M data sub-register banks, M constraint register sub-banks, and M equalizer FF weight register banks;

55. The fractional-spaced equalizer as set forth in claim **54** wherein said sampling factor M is equal to 2;

56. The fractional-spaced equalizer as set forth in claim **53** wherein said equalizer operates as a complex equalizer comprising complex operations;

57. The fractional-spaced equalizer as set forth in claim **53** wherein said equalizer operates as a real equalizer comprising real operations;

58. The fractional-spaced equalizer as set forth in claim **53** wherein said algorithm that computes the error associated with ISI cancellation is based upon a training sequence update and comprises:

a training sequence of distortion-less data; and

a differencing node to form the difference between the equalized decimated signal and the training sequence;

59. The fractional-spaced equalizer as set forth in claim **53** wherein said algorithm that computes the error associated with ISI cancellation is based upon a decision-directed update and comprises:

a slicer device to quantize samples of equalized decimated signal; and

a differencing node to form the difference between pre-slicer sequence and post-slicer sequence;

60. The fractional-spaced equalizer as set forth in claim **53** wherein said algorithm that computes the error associated with ISI cancellation is based upon the blind CMA update and comprises:

an algorithm to form the statistical parameter R_m measuring the ratio of moments of the pre-pulse shaped modulation amplitudes;

a switch S7 to eliminate the computation of R_m from the processing so that parameter R_m is computed only one time;

a register element to store the value of parameter R_m;

a complex conjugation operator to conjugate the sample input to the CMA;

a multiplier element to obtain the product between the input sample and its complex conjugate;

a differencing node to form the difference between parameter R_m and the absolute value of the input sample squared; and

a multiplier element to obtain the product of (1) the difference between parameter R_m and the absolute value of the input sample squared and (2) he input sample;

61. The fractional-spaced equalizer as set forth in claim **60** wherein said algorithm forming the value R_m comprises:

an absolute value operator to perform an absolute value of the input modulated 2-tuple;

a divide operation to form the value of R_m;

a switch S8 to control when the numerator portion of a ratio is to be delivered to the divide operation to form the value of parameter R_m;

a switch S9 to control when the denominator portion of a ratio is to be delivered to the divide operation to form the value of parameter R_m;

a counter to control when switches S8 and S9 are closed to form the value of parameter R_m;

a summing node used in the ratio's numerator accumulation process;

a summing node used in the ratio's denominator accumulation process;

a register element used in the ratio's numerator accumulation process;

a register element used in the ratio's denominator accumulation process;

a squaring operator;

a operator to perform a power operation to the m-th power; and

a parameter m representing the statistical moment of the CMA update satisfies the condition $m > 0$;

62. The fractional-spaced equalizer as set forth in claim **54** wherein said algorithm converting the ISI cancellation error signal into an adjustment signal comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input error sequence;

a parameter μ to control the adaptation rate of the equalizer's weight in accordance with the criterion for ISI cancellation; and

a multiplier element to form the product of the conjugated error sequence and parameter μ;

63. The fractional-spaced equalizer as set forth in claim **62** wherein the value for said scalar μ is in the range $0 < \mu < \mu_{crit}$ and μ_{crit} is inversely proportional to the power level of the samples of distorted waveform residing in the equalizer data register bank;

64. The fractional-spaced equalizer as set forth in claim **53** wherein said algorithm driving the equalizer weight update comprises:

a bank of multiplier elements to scale each element in the data register bank with a sample of the ISI cancellation adjustment signal; and

a bank of summing nodes to form the addition of the said bank of products with the current contents of the equalizer weight register bank;

65. The fractional-spaced equalizer as set forth in claim **53** wherein constraint waveform is defined to be a high frequency signal;

66. The fractional-spaced equalizer as set forth in claim **65** wherein said high frequency signal representing said constraint waveform is sinusoidal in nature;

67. The fractional-spaced equalizer as set forth in claim **66** wherein said high frequency sinusoid signal is a complex sinusoid of the form $A\ exp\{\ j\ 2\pi f\ kT_s + \phi\ \}$;

68. The fractional-spaced equalizer as set forth in claim **67** wherein said frequency *f* is a time variable frequency;

69. The fractional-spaced equalizer as set forth in claim **68** wherein minimum and maximum values of said time-variable frequency are selected to develop a robust out-of-band spectral mask for the FSE that is comparable to that of a MF;

70. The fractional-spaced equalizer as set forth in claim **67** wherein said amplitude A is an amplitude fixed to a singular value and satisfies $|A| > 0$;

71. The fractional-spaced equalizer as set forth in claim **67** wherein said amplitude A is a time variable amplitude and satisfies $|A| > 0$;

72. The fractional-spaced equalizer as set forth in claim **67** wherein said phase ϕ is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$;

73. The fractional-spaced equalizer as set forth in claim **67** wherein said phase ϕ is a time variable phase and satisfies $\{0 \leq \phi < 2\pi\}$;

74. The fractional-spaced equalizer as set forth in claim **66** wherein said high frequency sinusoid signal is a real sinusoid, either of the form $A\ sin\{\ 2\pi f\, kT_s + \phi\}$ or $A\ cos\{\ 2\pi f\, kT_s + \phi\}$;

75. The fractional-spaced equalizer as set forth in claim **74** wherein said frequency f of said sinusoid is a time variable frequency;

76. The fractional-spaced equalizer as set forth in claim **75** wherein minimum and maximum values of said time-variable frequency are selected to develop a robust out-of-band spectral mask for the FSE that is comparable to that of a MF;

77. The fractional-spaced equalizer as set forth in claim **74** wherein said amplitude A is an amplitude fixed to a singular value and satisfies $|A| > 0$;

78. The fractional-spaced equalizer as set forth in claim **74** wherein said amplitude A is a time variable amplitude and satisfies $|A| > 0$;

79. The fractional-spaced equalizer as set forth in claim **74** wherein said phase ϕ is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$;

80. The fractional-spaced equalizer as set forth in claim **74** wherein said phase ϕ_s is a time variable phase and satisfies $\{0 \leq \phi < 2\pi\}$;

81. The fractional-spaced equalizer as set for in claim **53** wherein said sinusoid representing said constraint waveform is generated via an algorithm comprising of:

an overflow counter to generate an integer i that indexes a frequency register bank;

a frequency register bank storing the independent frequencies of the sinusoidal signal representing the constraint waveform;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a parameter N representing the number of independent constraint frequencies;

a summing node to increment the count of the overflow counter; and

a quadrature oscillator that generates samples of the sinusoidal signal representing the constraint waveform from the frequencies in the frequency register bank;

82. The fractional-spaced equalizer as set for in claim **53** wherein samples of said sinusoidal constraint waveform are loaded into the constraint register bank via ROM lookup table;

83. The fractional-spaced equalizer as set forth in claim **53** wherein value of said constraint level parameter β resides in the range $\{0 \leq \beta < 1\}$;

84. The fractional-spaced equalizer as set forth in claim **53** wherein said differencing node forming constraint error is eliminated from the architecture of the present invention when parameter β is set to 0;

85. The fractional-spaced equalizer as set forth in claim **53** wherein said MF error adjustment algorithm comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input MF constraint error;

a parameter α to control the adaptation rate of the equalizer's weight in accordance with the MF constraint criterion; and

a multiplier element to form the product of the complex conjugate MF constraint error and parameter α;

86. The fractional-spaced equalizer as set forth in claim **85** wherein the value for said scalar α satisfies $\alpha > 0$;

87. The fractional-spaced equalizer as set forth in claim **86** wherein the value for said scalar α is equal to A/L commensurate with the constraint waveform defined as a sinusoidal signal of amplitude A and length L;

88. The fractional-spaced equalizer as set forth in claim **53** where said fractional-spaced equalizer further comprises an algorithm that modifies the constraint waveform via time-domain windowing;

89. The fractional-spaced equalizer as set forth in claim **88** wherein said an algorithm that modifies the constraint waveform via time-domain windowing does so with a single window function;

90. The fractional-spaced equalizer as set forth in claim **89** wherein said algorithm that modifies the constraint waveform via time domain windowing with a single window function comprises:

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a window function; and

a set of coefficients representing a window function used to window the samples of the constraint sinusoid; and

a bank of register elements to store the set of coefficients representing the window function;

91. The fractional-spaced equalizer as set forth in claim **90** wherein said window function is derived from any function that can modify the time response of the constraint sinusoid through time-domain windowing;

92. The fractional-spaced equalizer as set forth in claim **91** wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function;

93. The fractional-spaced equalizer as set forth in claim **88** wherein said an algorithm that modifies the constraint waveform via time domain windowing does so with multiple window functions;

94. The fractional-spaced equalizer as set forth in claim **93** wherein said an algorithm that modifies the constraint waveform via time domain windowing with multiple window functions comprises:

a register bank to store the samples of the current state of the windowed constraint waveform during the multi-window process;

a switch S10 to load the pre-windowed constraint waveform into the register bank only one time;

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a particular window function of the set of window functions;

a collection of window functions used to window the samples of the constraint sinusoid;

a collection of banks of register elements to store the set of coefficients of the collection of window functions;

a switch S12 to allow the multiplier bank to access a particular window function of the set of window functions; and

a switch S11 to deliver the windowed constraint waveform to the constraint register bank when the windowing process has been completed;

95. The fractional-spaced equalizer as set forth in claim **94** wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function;

96. The fractional-spaced equalizer as set forth in claim **53** where said fractional spaced equalizer further comprises an algorithm that controls the rate at which the contents of the equalizer's FF weight register bank are updated in accordance with the MF constraint update;

97. The fractional-spaced equalizer as set forth in claim **96** where said algorithm that controls the rate at which the contents of the equalizer's FF weight register bank are updated in accordance with the MF constraint update comprises:

a switch S3 to control when the algorithm for updating the contents of the equalizer FF weight registers is to be engaged;

an overflow counter to control when switch S3 is to be open and closed;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

a summing node to increment the count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a switch S4 to allow the overflow test to use the value designated by parameter P0 as the maximum count value;

a switch S5 to allow the overflow test to use the value designated by parameter P1 as the maximum count value;

a switch S6 to allow the overflow test to use the value designated by parameter P2 as the maximum count value;

a parameter P0 that represents a maximum count value;

a parameter P1 that represents a maximum count value; and

a parameter P2 that represents a maximum count value;

98. The fractional-spaced equalizer as set forth in claim **97** wherein said parameters P0, P1, and P2 are integers and satisfy $P0 > 0$, $P1 > 0$, and $P2 > 0$;

99. The fractional-spaced equalizer as set forth in claim **53** wherein said fractional spaced equalizer further comprises an algorithm that initializes the contents of the equalizer's FF weight register bank with coefficients of RRC MF;

100. The fractional-spaced equalizer as set forth in claim **99** where said algorithm that initializes the contents of the equalizer's FF weight register bank with coefficients of a RRC MF comprises:

a selected set of RRC MF coefficients loaded from ROM into the register positions of the equalizer FF weight register bank; and

a switch S13 to shutoff the initialization after the contents of the equalizer FF weight register bank;

101. The fractional-spaced equalizer as set forth in claim **53** where said fractional-spaced equalizer further comprises a decision-feedback update;

102. The fractional-spaced equalizer as set forth in claim **101** where said decision-feedback update comprises:

a register delay bank to store past decisions from a slicer device;

a slicer device to quantize samples of equalized decimated signal;

a register bank representing the decision register bank that stores the values of the weights of a decision-feedback filter;

a bank of multiplier elements used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a bank of summing nodes used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a single summing node adding the decision register and decision-feedback weight inner product to the output of the 2:1 commutator;

a bank of multiplier elements used in updating the contents of the decision-feedback weight register bank; and

a bank of summing nodes in updating the contents of the decision-feedback weight register bank;

103. A method of performing the inner product computation associated with the MF constraint criterion, the method comprising the steps of:

using only the L_w central multiplier elements of the multiplier bank, where $L_w < L$, to multiply only L_w central samples of the constraint waveform with the contents of only the L_w central registers of the equalizer FF weight register bank; and

using only the L_w central summing nodes of the bank of summing nodes, where $L_w < L$, to add up the L_w products formed from multiplication of only the L_w central samples of the constraint waveform with the contents of only the L_w central registers of the equalizer FF weight register bank;